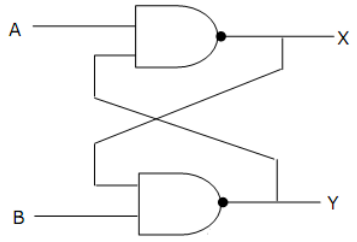
4 Sequential circuits

1. An SR latch is a :
   (A) combinational circuit
   (B) synchronous sequential circuit
   (C) one clock delay element
   (D) one bit memory element

2. An S-R flip-flop can be converted into a T flip flop by connecting X to $\overline{Q}$ and Y to Q. What are the values of X and Y?
   (A) S,R
   (B) R,S
   (C) $\overline{S}$, R
   (D) $S, \overline{R}$

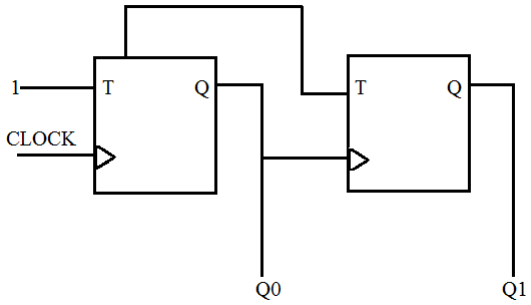
3. In the figure below A=1 and B=1 initially.



   The input B is now replaced with a sequence of bits as 10101010.... The output X and Y will be:
   (A) Fixed at 0 and 1 respectively
   (B) X=101010... while Y=010101...
   (C) X=101010... while Y=101010...
   (D) Fixed at 1 and 0 respectively

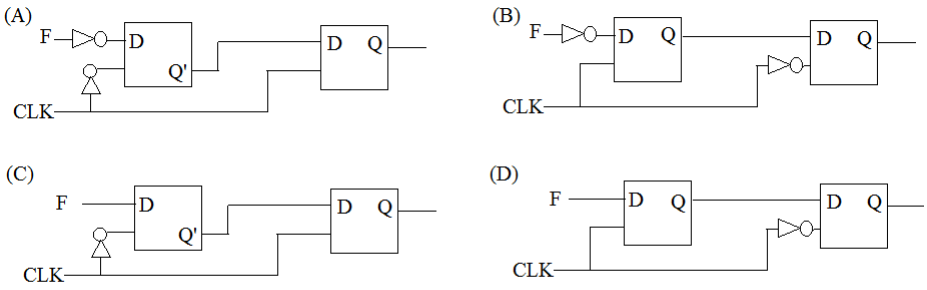
4. In an SR latch made by cross-coupling two NAND gates, if both S and R inputs are set to 0, then it will result in
   (A) Q = 0, Q' = 1
   (B) Q = 1, Q' = 0
   (C) Q = 1, Q' = 1
   (D) Indeterminate states

5. In the sequential circuit shown below,if the initial value of the output Q1Q0 is 00,what are the next four values of Q1Q0:



(A) 11,10,01,11
(B) 10,11,01,00
(C) 10,00,01,11
(D) 11,10,01,00

6. You are given a free running clock with a duty cycle of 50% and a digital waveform F which changes only at the negative edge of the clock. Which one of the following circuits (using clocked D flip-flops) will delay the phase of F by 180°?

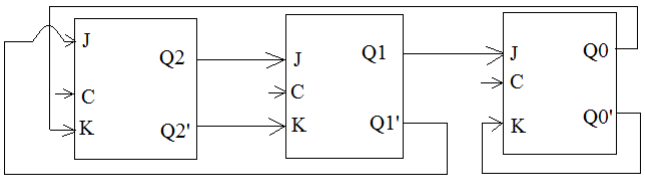


7. A Master-Slave flip-flop has the characteristic that:
(A) Change in input immediately reflected in the output.
(B) Change in output occurs when the state of Slave is affected.
(C) Change in output occurs when the state of Master is affected.
(D) Change of the output occurs when state of Both the Master and Slave are affected simultaneously.

8. The present output of an edge-triggered JK flip flop is said to be Q_n. If $Q_n = J' = 0$ then Q_{n+1} is:
(A) Cant be determined
(B) Will be logic-0

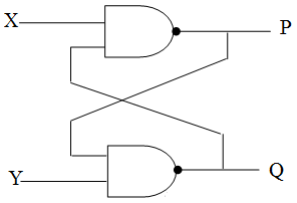
(C) Will be logic-1
(D) Will Race around

9. The above synchronous sequential circuit built using JK flip-flops is initialized with $Q_2Q_1Q_0 = 000$. The state sequence for this circuit for the next 3 clock cycles is



(A) 001, 010, 011
(B) 111, 110, 101
(C) 100, 110, 111
(D) 100, 011, 001

10. In the following circuit binary values were applied to the inputs X and Y inputs of the NAND latch shown in the figure in the sequence indicated below:
$X = 0 = Y'$;
$X = 0 = Y$;
$X = 1 = Y$;



The corresponding stable outputs at P and Q are:
(A) $P = 1 = Q'; P = 1 = Q'; P = 1 = Q'$ OR $P' = 1 = Q$
(B) $P = 1 = Q'; P = 0 = Q'$ OR $P' = 1 = Q$; $P = 0 = Q'$
(C) $P = 1 = Q'; P' = 0 = Q'; P = 1 = Q'$ OR $P' = 1 = Q$
(D) $P = 1 = Q'; P = 1 = Q; P' = 0 = Q'$;

11. Let $k = 2^n$. A circuit is built by giving the output of an n-bit Mod-n binary counter as input to an n-to-2^n bit decoder. This circuit is equivalent to a:
(A) k-bit binary up counter.
(B) n-bit binary down counter.
(C) k-bit ring counter.

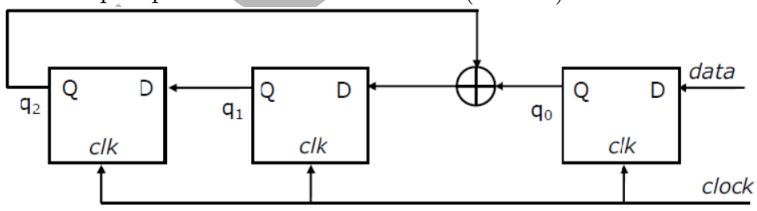
(D) 2k-bit Johnson counter.
(E) n-bit ring counter.

12. A pulse train can be delayed by a finite number of clock periods using a:
(A) Serial in serial out shift register
(B) Serial in parallel out shift register
(C) parallel in serial out shift register
(D) parallel in parallel out shift register

13. If in an UP counter each flip-flop is triggered by A and in a DOWN-counter, each flip-flop is triggered by B, what are the values of A ad B repectively?
(A) A = The output of the next flip-flop, B = The clock pulse of the previous flip-flop
(B) A = The normal output of the preceding flip-flop, B = The inverted output of the preceding flip-flop
(C) A = The clock pulse of the previous flip-flop, B = The output of the next flip-flop
(D) A = The inverted output of the preceding flip-flop, B = The normal output of the preceding flip-flop

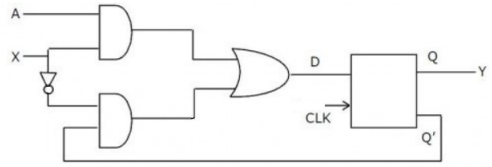
14. What is the preset condition for a ring counter?
(A) All flp flops set to 1
(B) All flp flops cleared to 0
(C) A single 0, the rest 1
(D) A single 1, the rest 0

15. Consider the circuit in the diagram. The $\oplus$ operator represents Ex-OR. The D flip-flops are initialized to zeroes (cleared).

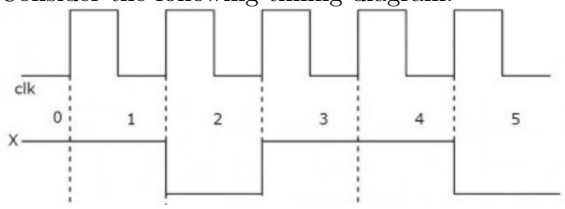


The following data: 100110000 is supplied to the "data" terminal in nine clock cycles. After that the values of $q_2 q_1 q_0$ are:
(A) 000
(B) 001
(C) 010
(D) 101

16. Consider the following circuit involving a positive edge triggered D FF.

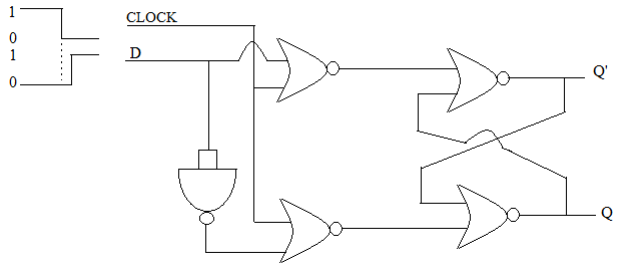


Consider the following timing diagram.



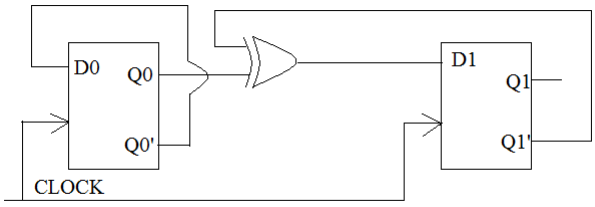
Let A_i represent the logic level on the line A in the i^{th} clock period and let A' represents complement of A.
The correct output sequence on Y over the clock periods 1 through 5 is
(A) A0 Al A1' A3 A4
(B) A0 Al A2' A3 A4
(C) Al A2 A2' A3 A4
(D) Al A2' A3 A4 A5'

17. For the circuit shown below D has the transition from 0 to 1 after clock changes from 1 to 0. Assume gate delays to be negligible.



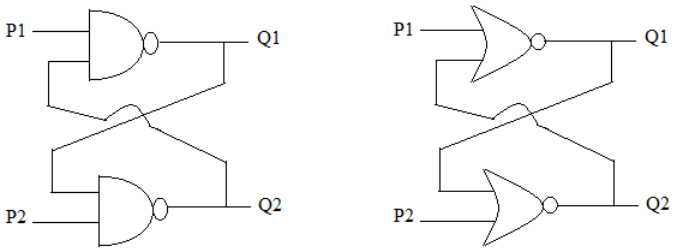
Which of the following statements is NOT FALSE?
(A) Q goes to 1 at the clock transition and stays at 1
(B) Q goes to 0 at the clock transition and stays at 0
(C) Q goes to 1 at the clock transition and goes to 0 when D does to 1
(D) Q goes to 0 at the clock transition and goes to 1 when D does to 1

18. Consider the following circuit.



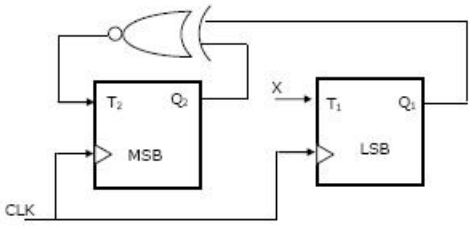
The flip-flops are positive edge triggered D FFs. Each state is designated as a two bit string Q0Q1. Let the initial state be 00. The state transition sequence is:
(A) 00,10,11,00,10
(B) 00,11,10,00,11
(C) 00,11,01,10,00
(D) 00,10,01,11,00

19. Refer to the NAND and NOR latches show below. The inputs (P_1, P_2) for both the latches are first made (0,1) and then after a few seconds made (1,1) respectively.



The corresponding stable outputs (Q_1, Q_2) are:
(A) NAND: first(0,1) then (0,1); NOR:first(1,0) then (0,0);
(B) NAND: first(1,0) then (1,0); NOR:first(1,0) then (1,0);
(C) NAND: first(1,0) then (1,0); NOR:first(1,0) then (0,0);
(D) NAND: first(1,0) then (1,1); NOR:first(0,1) then (0,1);

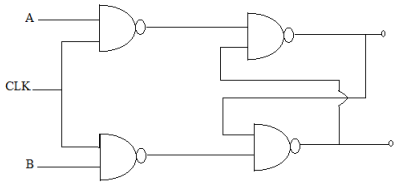
20. Consider the partial implementation of a 2-bit counter using T flip-flops following the sequence 0-2-3-1-0 as shown below.



To complete the circuit, the input X should be:

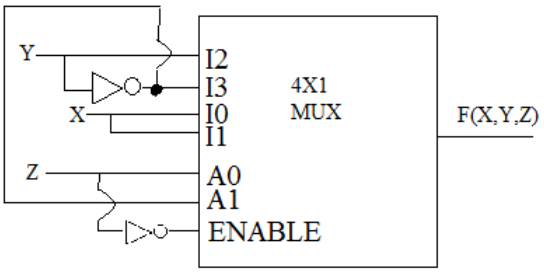
(A) $\overline{Q_2}$
(B) $Q_2 + Q_1$
(C) $\overline{(Q_1 + Q_2)}$
(D) $Q_1 \oplus Q_2$

21. Consider the circuit show below.



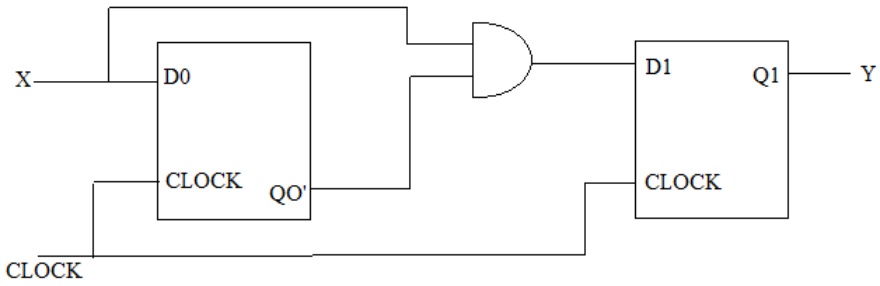
In the circuit the condition of RACE around:
(A) does not occur
(B) occurs when CLK=0
(C) occurs when CLK=1 and A=B=1
(D) occurs when CLK=1 and A=B=0

22. Consider the following multiplexer where I0, I1, I2, I3 are four data input lines selected by two address line combinations A_1A_0 = 00, 01, 10, 11 respectively. The function F(X,Y,Z) implemented by the above circuit is:

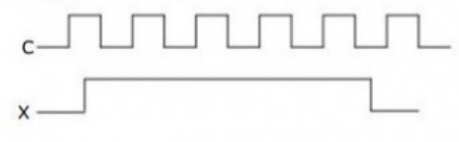


the above circuit is :
(A) XYZ'
(B) XY + Z
(C) X + Z
(D) None of the above

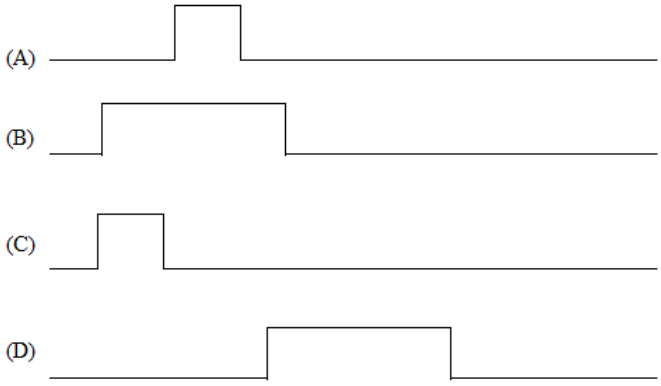
23. Consider the following circuit with initial state $Q_0 = Q_1 = 0$. The D Flip-flops are positive edged triggered and have set up times 20 nanosecond and hold times 0.



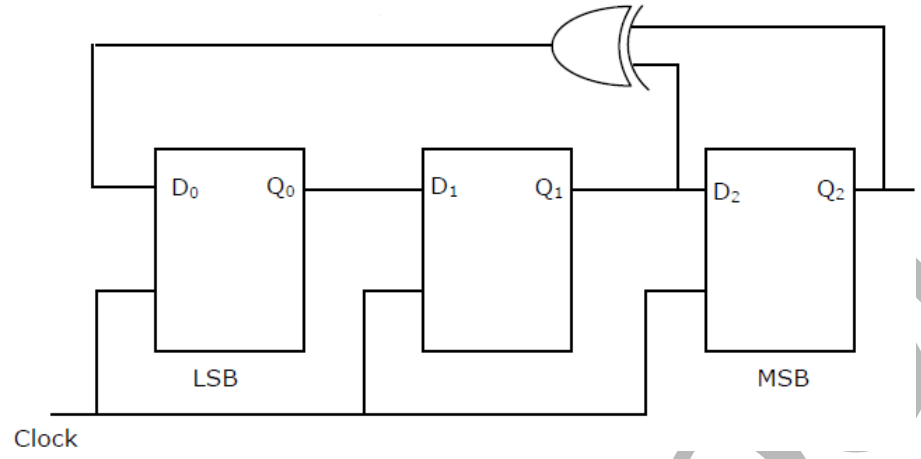
Consider the following timing diagrams of X and C. The clock period of $C \geq 40$ nanosecond.



Which one is the correct plot of Y?

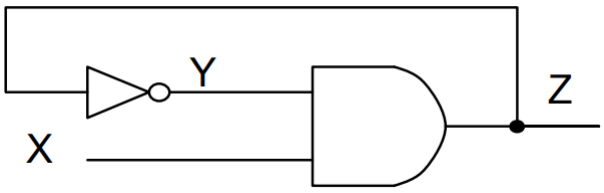


24. Consider the circuit given below with initial state Q0 =1, Q1 = Q2 = 0. The state of the circuit is given by the value 4Q2 + 2Q1 + Q0



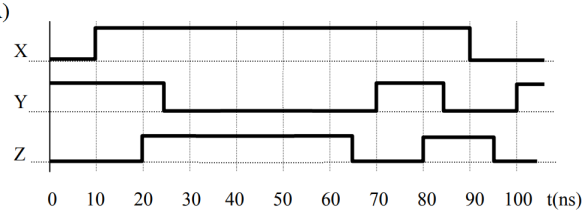
Which one of the following is the correct state sequence of the circuit?
(A) 1,3,4,6,7,5,2
(B) 1,2,5,3,7,6,4
(C) 1,2,7,3,5,6,4
(D) 1,6,5,7,2,3,4

25. Assume that the inverter in the network below has a propagation delay of 5 ns and the AND gate has a propagation delay of 10 ns.
Let TD be the timing diagram for the network showing X, Y, and Z below. Assume that X is initially 0, Y is initially 1, X becomes 1 for 80 ns, and then X is 0 again.

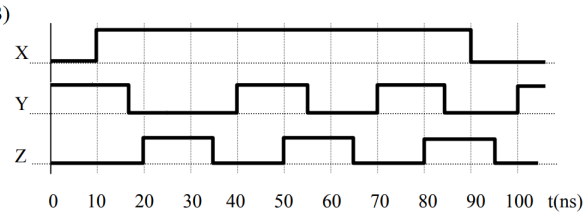


Which of the following depicts TD most appropriately:

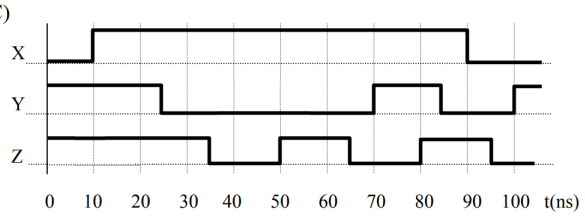
(A)



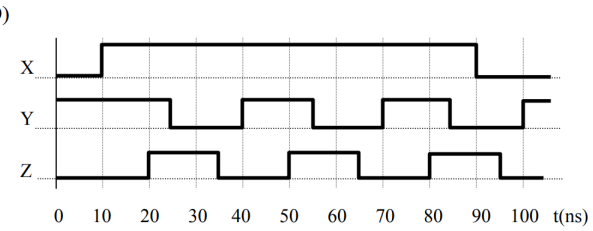
(B)



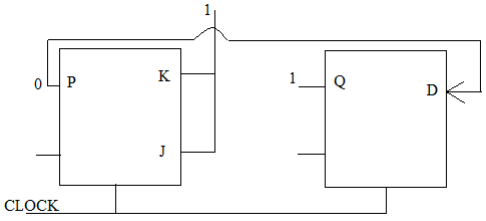
(C)



(D)



26. The following arrangement of master-slave flip flops has the initial state of P=0 and Q=1.



After three clock cycles, states of the output P, Q is respectively are:
(A) 1,1
(B) 0,1
(C) 1,0
(D) 0,0

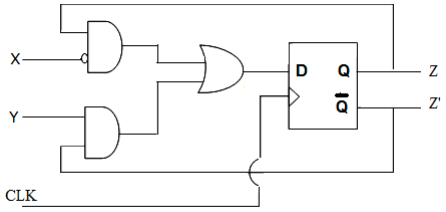
27. A positive edge-triggered D flip-flop is connected to a positive edge-triggered JK flipflop as follows. The Q output of the D flip-flop is connected to both the J and K inputs of the JK flip-flop, while the Q output of the JK flip-flop is connected to the input of the D flip-flop. Initially, the output of the D flip-flop is set to logic one and the output of the JK flip-flop is cleared. Which one of the following is the bit sequence (including the initial state) generated at the Q output of the JK flip-flop when the flip-flops are connected to a free-running common clock? Assume that J = K = 1 is the toggle mode and J = K = 0 is the state-holding mode of the JK flip-flop. Both the flip-flops have non-zero propagation delays.
(A) 0110110...
(B) 0100100...
(C) 011101110...
(D) 011001100..

28. Consider a 4 bit Johnson counter with an initial value of 0000. The counting sequence of this counter is:
(A) 0, 1, 3, 7, 15, 14, 12, 8, 0
(B) 0, 1, 3, 5, 7, 9, 11, 13, 15, 0
(C) 0, 2, 4, 6, 8, 10, 12, 14, 0
(D) 0, 8, 12, 14, 15, 7, 3, 1, 0

29. The minimum number of JK flip-flops required to construct a synchronous counter with the count sequence (0, 0, 1, 1, 1, 2, 1, 2, 1, 3, 3, 0, 0, 1, 1, 1, 2, 1, 2, 1, 3, 3, 0, 0...) is:
(A) 3
(B) 4
(C) 5
(D) 6
(E) 7

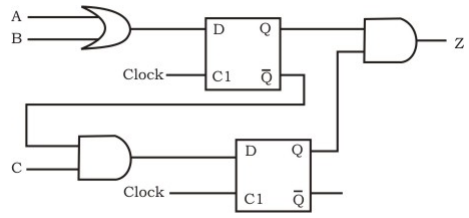
30. How many pulses are needed to change the contents of a 8-bit up counter from 10101100 to 00100111?
(A) 134
(B) 133
(C) 124
(D) 123

31. A sequential circuit using D flip flop and logic gates is shown in the figure below.



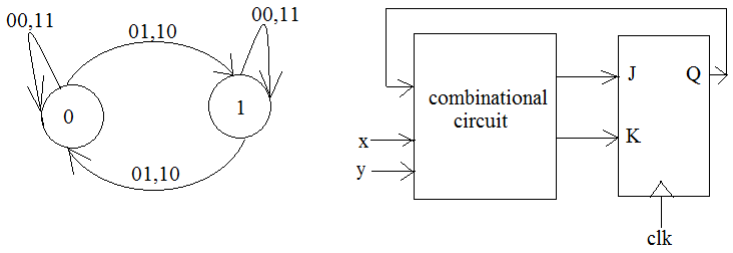
The circuit is:
(A) SR flip flop with X=R and Y=S
(B) SR flip flop with X=S and Y=R
(C) JK flip flop with X=J and Y=K
(D) JK flip flop with X=K and Y=J

32. Which of the following input sequences will always generate a 1 at the output z at the end of the third cycle?



(A) 0,0,0,1,0,1,1,1,1
(B) 1,0,1,1,1,0,1,1,1
(C) 0,1,1,1,0,1,1,1,1
(D) 0,0,1,1,1,0,1,1,1

33. Consider the following state diagram and its realization by a JK flip flop.

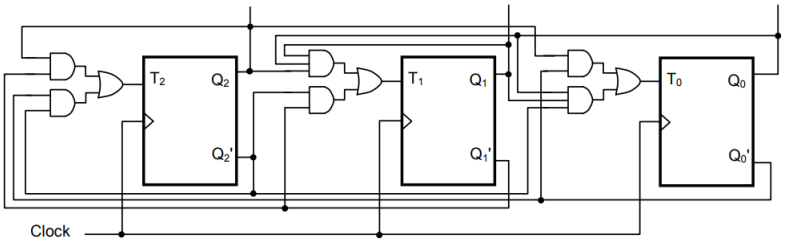


The combinational circuit generates J and K in terms of x, y and Q. The Boolean expressions for J and K are :

(A) $\overline{x \oplus y}$ and $\overline{x} \oplus \overline{y}$
(B) $\overline{x \oplus y}$ and $x \oplus y$
(C) $x \oplus y$ and $\overline{x \oplus y}$
(D) $x \oplus y$ and $x \oplus y$

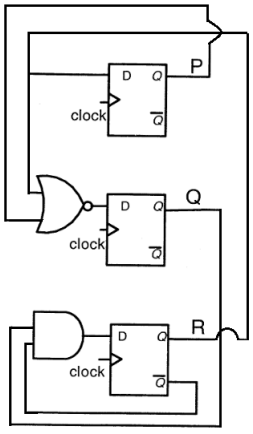
34.

35. Consider the following figure depicting a counter using only T flip flops and 2-input AND and OR gates:



Q_0, Q_1 and Q_2 are the output which are probed for the counter's states with input clock.
Which of the following sequence of states belongs to this counter?
(A) 001, 011, 010, 100, 110, 101, 001
(B) 000, 001, 010, 100, 110, 101, 001
(C) 000, 001, 010, 110, 111, 101, 001
(D) 001, 011, 010, 110, 111, 101, 001

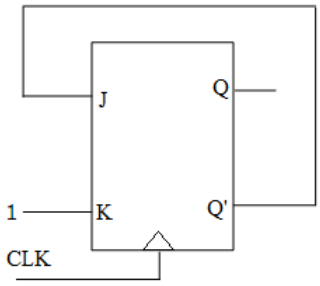
36. Consider the following circuit involving three D-type flip-flops used in a certain type of counter configuration.



If at some instance prior to the occurrence of the clock edge, P,Q and R have a value 0, 1 and 0 respectively, what shall be the value of PQR after the clock edge?

(A) 000
(B) 001
(C) 010
(D) 011

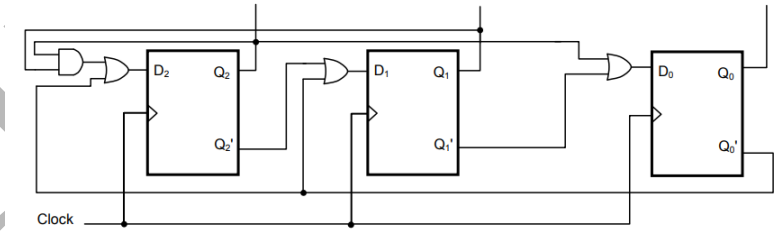
37. Consider the following circuit shoen below:



The JK flip flop has, $J = Q'$ and $K = 1$. Assume the flip flop was initially cleared and then clocked for 6 pulses.
Then the sequence at the output will be:
(A) 010000
(B) 011001
(C) 010010
(D) 010101

38. A switch-tail ring counter is made using a single D flip flop. The resulting circuit is equivalent to:
(A) SR flip flop
(B) JK flip flop
(C) D flip flop
(D) T flip flop

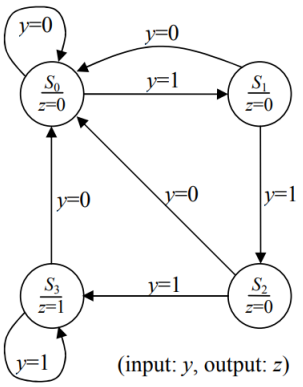
39. Consider the following figure depicting a counter using only D flip flops:



Q_0, Q_1 and Q_2 are the output which are probed for the counter's states with input clock.
Which of the following sequence of states belongs to this counter?

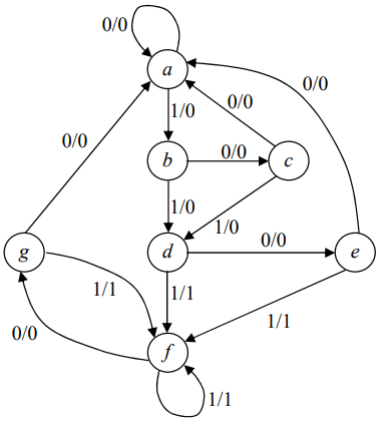
(A) 001, 011, 010, 100, 110, 101, 001
(B) 000, 001, 010, 100, 110, 101, 001
(C) 000, 001, 010, 110, 111, 101, 001
(D) 001, 011, 010, 110, 111, 101, 001

40. Consider the finite state diagram shown below followed by some statement:



(i) The diagram resembles a Mealy model which detects any bit string of length ≥ 3.
(ii) The diagram resembles a Moore model which detects any sequence of consecutive 1's with length at most 3.
(iii) The diagram resembles a Mealy model which detects any sequence of 3 or more consecutive 1's.
(iv) The diagram resembles a Moore model which detects any sequence of 3 or more consecutive 1's.

41. Consider the state transition diagram show below:



Which of the following table shows the function of above diagram most

appropriately:

(A)

Present state	Next state $x=0$	Next state $x=1$	Output $x=0$	Output $x=1$
a	a	b	0	0
b	c	d	0	0
c	a	d	1	0
d	e	a	0	1
e	a	d	0	1

(B)

Present state	Next state $x=0$	Next state $x=1$	Output $x=0$	Output $x=1$
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	d	0	1
e	a	a	0	1

(C)

Present state	Next state $x=0$	Next state $x=1$	Output $x=0$	Output $x=1$
a	a	b	0	0
b	c	d	0	0
c	a	d	1	0
d	e	d	0	1
e	a	a	0	1

(D)

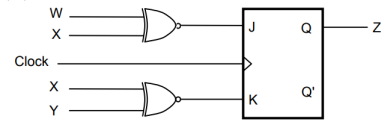
Present state	Next state $x=0$	Next state $x=1$	Output $x=0$	Output $x=1$
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	d	0	1
e	a	d	0	1

42. Consider the following state table:

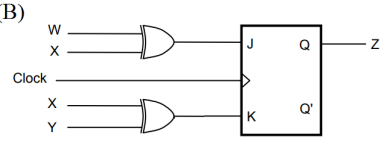
	Input (WXY =) 000	001	010	011	100	101	110	111	Output Z =
a	a	a	b	b	b	b	a	a	0
b	a	b	b	a	a	b	b	a	1

Which of the following sequential circuits realizes the table described above:

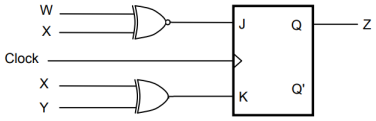
(A)



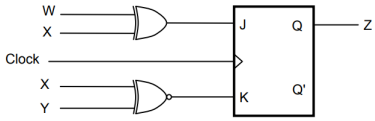
(B)



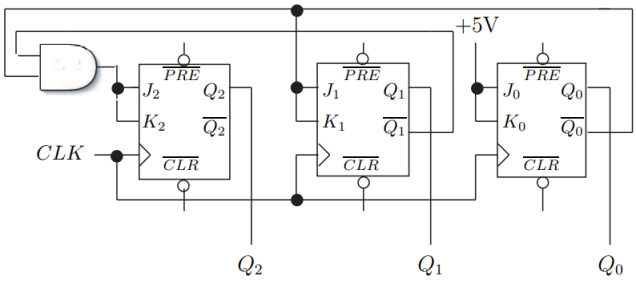
(C)



(D)



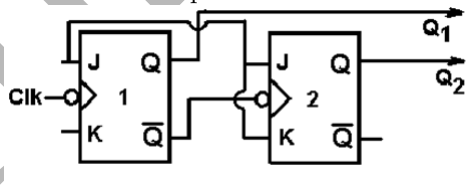
43. Consider the sequential circuit shown below. It uses 3 J-K flip flops and an AND gate (fan-in = 2). $Q_0Q_1Q_2$ are its outputs. CLR and PRE are clear and Preset lines working at active low mode.



Which of the following represents the functioning of this sequential circuit?

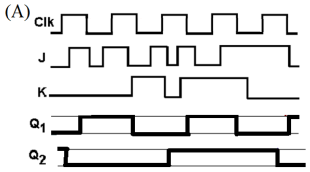
(A) 3-bit binary asynchronous up-counter
(B) 3-bit binary synchronous down-counter
(C) 3-bit binary asynchronous down-counter
(D) 3-bit binary synchronous up-counter

44. Consider the sequential circuit below using JK flip flop:

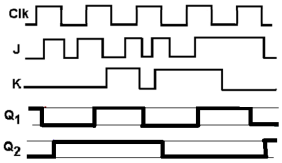


Which of the following timing diagram is a correct representation of the circuit above:

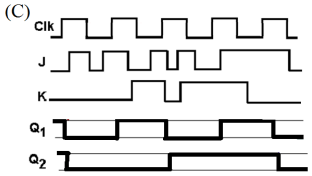
(A)



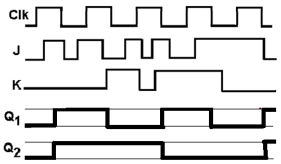
(B)



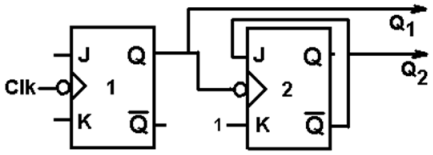
(C)



(D)

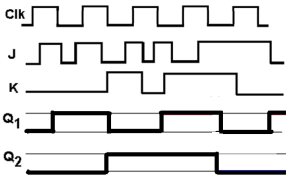


45. Consider the sequential circuit below using JK flip flop:

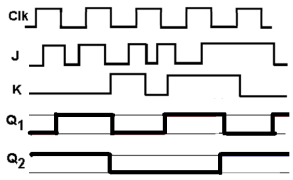


Which of the following timing diagram is a correct representation of the circuit above:

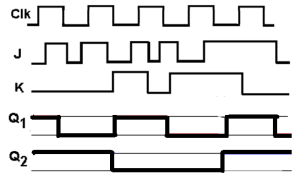
(A)



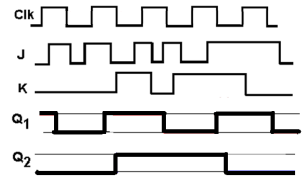
(B)



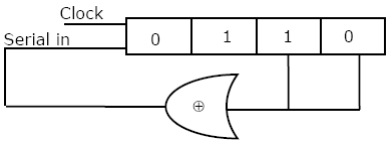
(C)



(D)

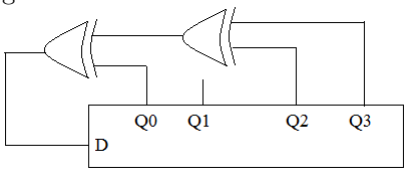


46. The initial content of the 4 bit serial in serial out right shifting shift register shown in the figure is 0110. After three clock pulses are applied the content of the shift register will be:



(A) 0000
(B) 0101
(C) 1010
(D) 1111

47. A 4 bit shift register, which shifts 1 bit to the right at every clock pulse, is initialized to values $Q_0Q_1Q_2Q_3 = 1000$. D is the serial input to this register as shown below:



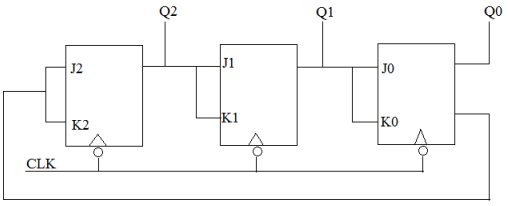
After how many clock pulses the initial pattern reappears?
(A) 8
(B) 6
(C) 12
(D) 5

48. Match the columns appropriately:

Group 1	**Group 2**
P: Shift Register	1: Frequency division
Q: Counter	2: Addressing in memory chips
R: Decoder	3: Serial to Parallel data conversion

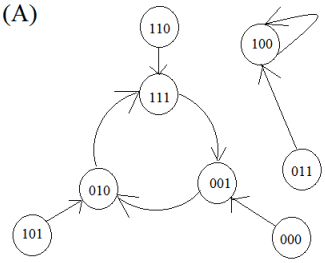
(A) P-3, Q-2, R-1
(B) P-3, Q-1, R-2
(C) P-2, Q-1, R-3
(B) P-1, Q-2, R-2

49. Consider the circuit below:

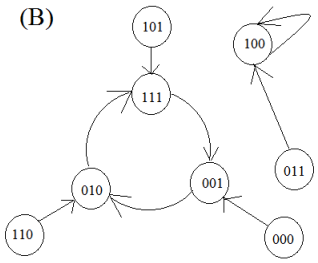


Which of the following count sequence diagram represents the functioning of the counter circuit above:

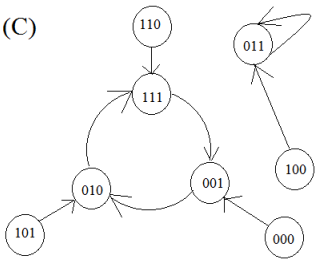
(A)



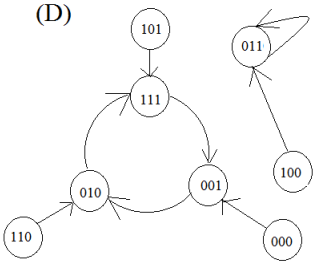
(B)



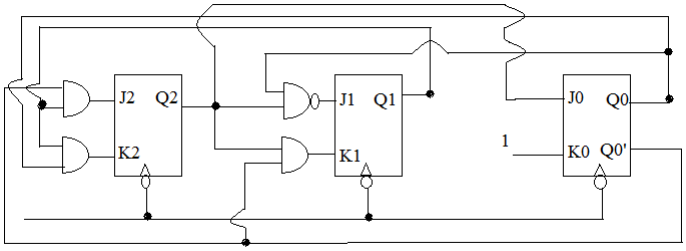
(C)



(D)



50. Consider the following sequential circuit to be employed as a counter.



Which if the following state sequence belongs to this counter?
(A) 1,2,3,5,6,7,1
(B) 2,3,5,6,7,0,2
(C) 2,3,5,1,7,2
(D) 1,2,6,3,5,1