3 Combinational Circuits

1. In a combinational circuit, the output at any time depends only on:
   (A) Applied Voltage
   (B) Intermediate values (C) Input values
   (D) Clock

2. When a condition in a program is to be tested which of the following is used to let the processor know if to go for next round or not?
   (A) General purpose register
   (B) Accumulator register
   (C) Program counter register
   (D) Program status word register

3. Indicate which of the following logic gates can be used to realize all possible combinational logic functions:
   (A) OR gates
   (B) AND gates
   (C) NAND gates
   (D) Ex-OR gates

4. The minimal function that can detect a "divisible by 3" 8421 BCD code digit (representation $D_8D_4D_2D_1$) is given by:
   (A) $D_8D_1 + D_4D_2 + \overline{D_8}D_2D_1$
   (B) $D_8D_1 + D_4D_2\overline{D_1} + \overline{D_4}D_2D_1 + \overline{D_8}.\overline{D_4}.\overline{D_2}.\overline{D_1}$
   (C) $D_8D_1 + D_4D_2 + \overline{D_8}.\overline{D_4}.\overline{D_2}.\overline{D_1}$
   (D) $D_4D_2\overline{D_1} + D_4D_2D_1 + D_8\overline{D_4}D_2D_1$

5. A combinational circuit has three inputs A, B and C and an output F. F is true only for the following combinations of inputs:

A=0	B=1	
A=0		C=1
A=1	B=1	C=1
A=0	B=0	C=0

   Then answer the following questions:
   (i) Write the complete truth table for F.
   (ii) Write simplified expression for F as sum of products and product of sums format.
   (iii) Draw the logic circuit of F using minimum number of 2-inputs NAND

gates.

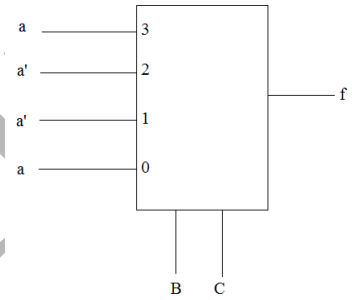
6. A 2-bit binary multiplier can be implemented using :
   (A) 2-input AND gates only
   (B) 2-input Exor gates and 2-input AND gates only
   (C) Two 2-input NOR gates and one Exor gate
   (D) Exor gates and shift registers

7. If A and B are the inputs to a half adder, the expression for pair (sum,carry) is given by
   (A) (A AND B, A AND B)
   (B) (A OR B, A OR B)
   (C) (A $\oplus$ B, A OR B)
   (D) (A $\oplus$ B, A AND B)

8. The number of fill and half-address required to add 16-bit number is:
   (A) 8 half-adders, 8 full-adders
   (B) 1 half-adder, 15 full-adders
   (C) 16 half-adders, 0 full-adders
   (D) 4 half-adders, 12 full-adders

9. If A, B and C are the inputs of a full adder then the expression for pair (sum,carry) is given by:
   (A) (A AND B AND C, A AND B+C_{in} AND (A $\oplus$ B))
   (B) (A $\oplus$ B OR C, B AND C+C_{out} AND (A $\oplus$ B))
   (C) (A $\oplus$ B $\oplus$ C, A AND B+C_{in} AND (A $\odot$ B))
   (D) (A $\oplus$ B $\oplus$ C, A AND B+C_{in} AND (A $\oplus$ B))

10. The Boolean expression for the output f of the 4x1 multiplexer shown below is:

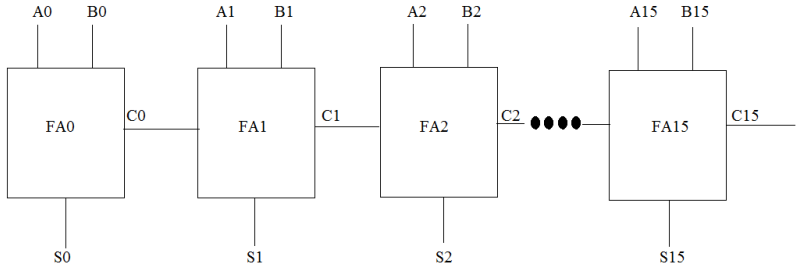


   (A) a$\odot$B$\odot$C

(B) $\overline{a \odot B \odot C}$
(C) B+C
(D) B.C

11. If only half adders are allowed to be used for adding two m bit numbers, then the number of half adders needed is:
(A) $2m - 1$
(B) $2^m - 1$
(C) $2^m + 1$
(D) $2m$

12. A 16 bit ripple carry adder is realized using 16 identical full adders (FA) as shown in the figure. The carry propagation delay of each of FA is 12 ns and the sum propagation delay of each of FA is 15 ns.The worst case delay, in ns, of this 16 bit adder will be:



(A) 240ns
(B) 192ns
(C) 195ns
(D) 237ns

13. The addition of A and B in a half Adder can be implemented by using K two-input NAND gates. The value of K is:
(A) 3
(B) 4
(C) 5
(D) 6

14. Let A and B is the input of a half subtractor then the output as a pair (difference, borrow) will be:
(A) $A \odot B$,$\overline{A}$ AND $\overline{B}$
(B) A $\odot$ B, $\overline{A}$ AND B
(C) A $\oplus$ B, $\overline{A}$ AND $\overline{B}$

(D) $A \oplus B$,$\overline{A}$ AND B

15. The full subtractor can be implemented using
(A) Two XOR and an OR gates
(B) Two half subtractors and an OR gate
(C) Two multiplexers and an AND gate
(D) None of the Mentioned

16. The Difference output of a full subtractor is same as:
(A) Sum output of a Half adder
(B) Sum output of a Full adder
(C) Difference output of a Half subtractor
(D) None of the above

17. The output Y of a 2-bit comparator is logic-1 whenever a 2-bit input A is greater than the 2-bit input B. The probability that the output is at logic-1 is:
(A) 0.25
(B) 0.375
(C) 0.50
(D) 0.625

18. Carry lookahead logic uses the concepts of
(A) Inverting the inputs
(B) Complementing the outputs
(C) Generating and propagating carries
(D) Ripple factor

19. What is a disadvantage of the ripple-carry adder?
(A) The interconnections are more complex
(B) More stages are required
(C) It is slow due to propagation time
(D) All of the above

20. A 4-bit carry lookahead adder, which adds two 4-bit numbers, is designed using AND, OR, NOT, NAND, NOR gates only. Assuming that all the inputs are available in both complemented and uncomplemented forms and the delay of each gate is one time unit, what is the overall propagation delay of the adder? Assume that the carry network has been implemented using two-level AND-OR logic.
(A) 4 time units
(B) 6 time units

(C) 10 time units
(D) 12 time units

21. Consider a carry look ahead adder for adding two n-bit integers, built using gates of fan-in at most two. The time to perform addition using this adder is:
(A) $\theta(1)$
(B) $\theta(Log(n))$
(C) $\theta(n^{0.5})$
(D) $\theta(n)$

22. Consider an eight-bit ripple-carry adder for computing the sum of A and B, where A and B are integers represented in 2's complement form. If the decimal value of A is one, the decimal value of B that leads to the longest latency for the sum to stabilize is:
(A) -1
(B) 2
(C) 1
(D) -2

23. In a look-ahead carry generator, the carry generate function G_i and the carry propagate function P_i for inputs A_i and B_i are given by:
$P_i = A_i \oplus B_i$ and $G_i = A_i.B_i$.
The expressions for the sum bit S_i and the carry bit C_{i+1} of the look-ahead carry adder are given by:
$S_i = P_i \oplus C_i$ and $C_{i+1} = G_i + P_i.C_i$, where C_0 is the input carry.
Consider a two-level logic implementation of the look-ahead carry generator. Assume that all P_i and G_i are available for the carry generator circuit and that the AND and OR gates can have any number of inputs. The number of AND gates and OR gates needed to implement the look-ahead carry generator for a 4-bit adder with S_3, S_2, S_1, S_0 and C_4 as its outputs are respectively:
(A) 6, 3
(B) 10, 4
(C) 6, 4
(D) 10, 5

24. In a 4-bit carry look ahead adder the propagation delay of Ex-OR gate is 20ns while the same of AND and OR gates is 10ns. The sum and carry output of full adder takes 20ns and 10ns respectively. The total propagation delay of the above adder in ns is:
(A) 50ns
(B) 60ns

(C) 70ns
(D) 80ns

25. If you are asked to design a 1-bit full adder using only 2-input NAND gates, how many gates would you like to budget in order to minimize the cost?
(A) 5
(B) 7
(C) 8
(D) 9
(E) 12

26. We are given 1-bit full adders which uses only 2-input NAND gates. A 4-bit Full adder is designed using these 1 bit Full adder and it is known that each NAND gate has 1 unit gate delay. Using these 4 bit full adders a 32 bit ripple carry adder is designed. What will be the total delay of this 32-bit ripple-carry adder if each gate delay is equivalent to 2 ns.
(A) 96ns
(B) 192ns
(C) 284ns
(D) 292ns
(E) 384ns
(F) None of the above

27. An $n*n$ array multiplier takes two n-bit inputs and produces the product of the two numbers at output. A logic-circuitry of an $n*n$ array multiplier uses only full adders and AND gates.
Which of the following pairs represents the correct expression for the pair (A,B), where A and B are number of 2-input AND gates and number of full adders, respectively, required to build the multiplier.
(A) $(n*n, n^2-n)$
(B) $((n-1)*n, n^2-2n)$
(C) $(n*n, n^2-2n)$
(D) $(n*n, n-1)$

28. Which of the following are building blocks of encoders?
(A) NOT gate
(B) Ex-OR gate
(C) AND gate
(D) NAND gate

29. How many outputs will a decimal-to-BCD encoder have?
(A) 4

(B) 9
(C) 10
(D) 16

30. How many multi-input OR gates are required for a ASCII-to-binary encoder?
(A) 127
(B) 63
(C) 15
(D) 7
(E) 1

31. In the following truth table, V = 1 if and only if the input is valid.

Inputs				Outputs		
D_0	D_1	D_2	D_3	X_0	X_1	V
0	0	0	0	x	x	0
1	0	0	0	0	0	1
x	1	0	0	0	1	1
x	x	1	0	1	0	1
x	x	x	1	1	1	1

What function does the truth table represent?
(A) Priority encoder
(B) Decoder
(C) Multiplexer
(D) Demultiplexer

32. How many 4-to-16 line decoders with an enable input are needed to construct a 8-to-256 line decoder without using any other logic gates?
(A) 9
(B) 11
(C) 16
(D) 17

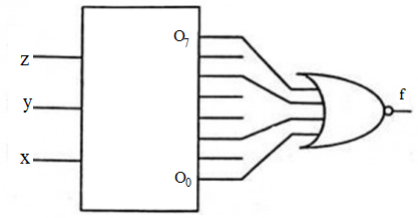
33. Number of AND gates required to realize a $\log n$Xn decoder for n being an integer equivalent to some power of 2:
(A) $n \log n$
(B) n^2
(C) 2^n
(D) $n - 1$
(E) n

34. A circuit outputs a digit in the form of 4 bits. 0 is represented by 0000, 1 by 0001, ..., 9 by 1001. A combinational circuit is to be designed which takes these 4 bits as input and outputs 1 if the digit ≥ 5, and 0 otherwise. If only AND, OR and NOT gates may be used, what is the minimum number of gates required?
(A) 2
(B) 3
(C) 4
(D) 5

35. Consider a *9 X 512* decoder circuit built using *3 X 8* decoders. A chip is to be designed which functions as a *27 X 134217728* decoder. What is the equivalent number of *3 X 8* decoder units involved in this chip?
(A) 134217728
(B) 262657
(C) 2101256
(D) 19136512
(E) 262730

36. Consider the following combinational function block involving four Boolean variables x, y, a, b where x, a, b are inputs and y is the output.
f(x,y,a,b)
{
if (x == 1) y = a;
else y = b;
}
Which one of the following digital logic blocks is the most suitable for implementing this function?
(A) Full adder
(B) Priority encoder
(C) Multiplexer
(D) Flip-flop

37. What Boolean function does the circuit below realize?



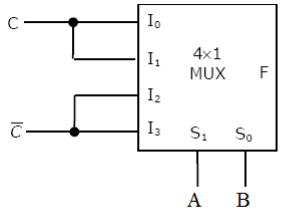
(A) xz+x'z'
(B) xz'+x'z

(C) x'y'+yz
(D) xy+y'z'

38. Consider a multiplexer with X and Y as data inputs and Z as control input. Z = 0 selects input X, and Z = 1 selects input Y. What are the connections required to realize the 2-variable Boolean function f = T + R, without using any additional hardware?
(A) R to X, 1 to Y, T to Z
(B) T to X, R to Y, T to Z
(C) T to X, R to Y, 0 to Z
(D) R to X, 0 to Y, T to Z

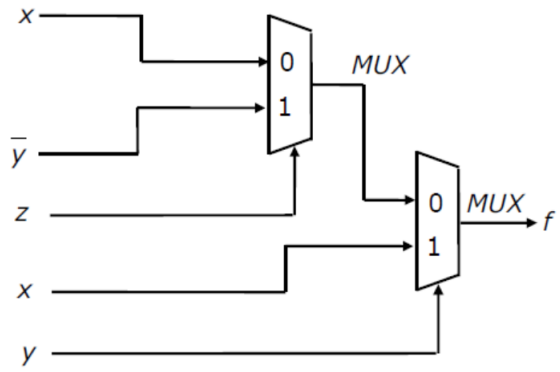
39. Suppose only one multiplexer and one inverter are allowed to be used to implement any Boolean function of n variables. What is the minimum size of the multiplexer needed?
(A) 2^n line to 1 line
(B) 2^{n+1} line to 1 line
(C) 2^{n-1} line to 1 line
(D) 2^{n-2} line to 1 line

40. The logic realized by the circuit shown in the figure is:



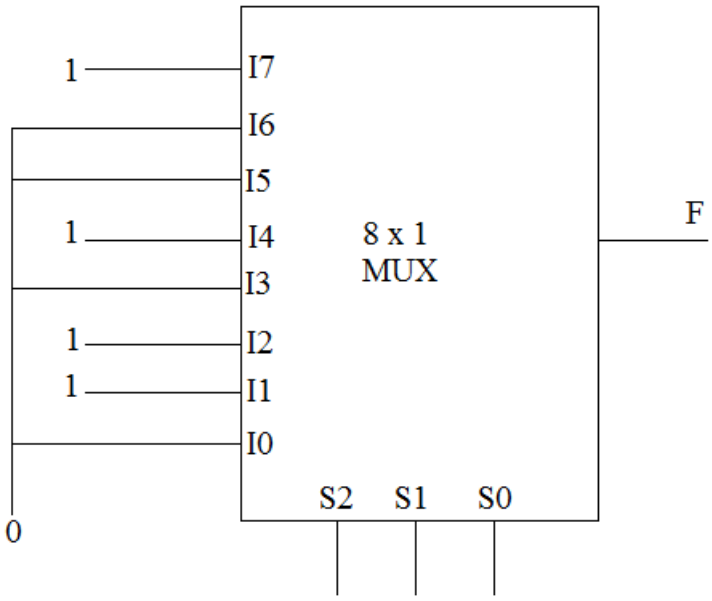
(A) F = A.C
(B) F = A⊕C
(C) F = B⊕C
(D) F = B⊙C
(E) F = A+C

41. Consider the circuit shown below.



Which one of the following options correctly represents f(x,y,z)?
(A) $x\overline{z} + xy + \overline{y}z$
(B) $x\overline{z} + xy + \overline{(yz)}$
(C) $xz + xy + \overline{(yz)}$
(D) $xz + x\overline{y} + \overline{y}z$

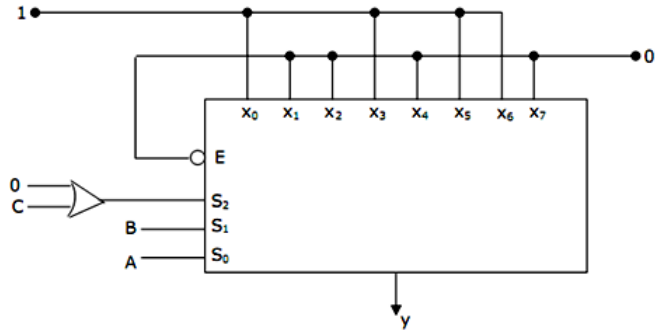
42. Consider the 8x1 multiplexer shown below:



What function does the multiplexer represent?
(A) Carry output of a Full adder
(B) Partial product of an array multiplier

(C) Sum output of a Half adder
(D) Carry output of a Half adder
(E) A difference output of a Full subtractor

43. In the circuit shown in below figure, S_2, S_1 and S_0 are select lines and X_i are input lines where $i \in N$ and $0 \leq i \leq 7$. S_2 and X_7 are MSBs. The output Y is:



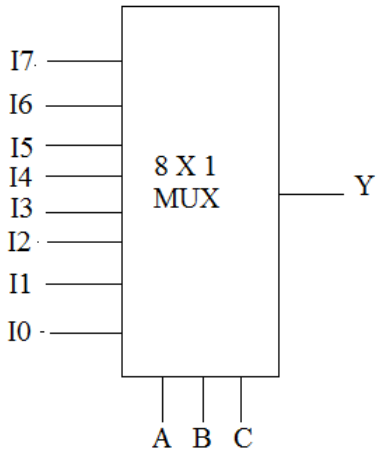
(A) $A \oplus B$
(B) $A \odot B$
(C) $\overline{C}.\overline{A \oplus B} + C.(A \oplus B)$
(D) Indeterminate

44. Without any additional circuitry an 8:1 MUX can be used to obtain:
(A) Some but not all Boolean functions of three variables.
(B) All functions of three variables but none of four variables.
(C) All functions of three variables and some of four variables.
(D) All functions of four variables.

45. Consider the function F(A,B,C,D) shown in the figure below:

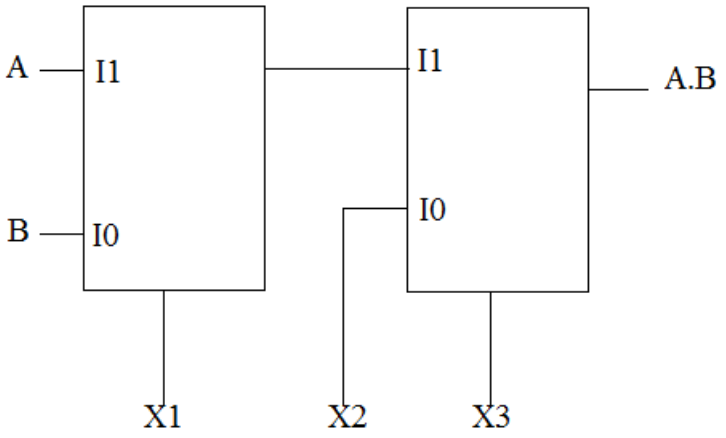
F(A,B,C,D)

A	B	C	D	F( )
0	0	0	0	1
0	0	0	1	1
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	0	0	1
1	1	1	1	1



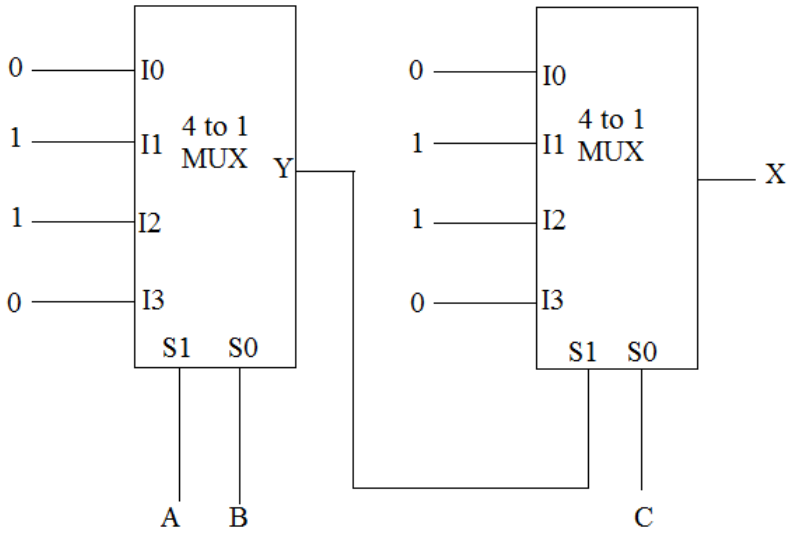
In order to realize $Y = F$ on an 8X1 MUX (shown in the figure) what should be the set of inputs to MUX as a tuple $(I_0, I_1, I_2, I_3, I_4, I_5, I_6, I_7)$:
(A) $(1, 0, 0, D, \overline{D}, 0, 0, 1)$
(B) $(1, 0, 0, \overline{D}, D, 0, 0, 1)$
(C) $(1, 0, D, \overline{D}, 0, 1, 0, 1)$
(D) $(1, 0, 0, D, \overline{D}, 0, 1, 1)$

46. The following circuit implements a two-input AND gate using two 2-1 multiplexers.



What are the values of X1,X2,X3?
(A) X1=B,X2=0,X3=A
(B) X1=B,X2=1,X3=B
(C) X1=A,X2=B,X3=1
(D) X1=A,X2=0,X3=B

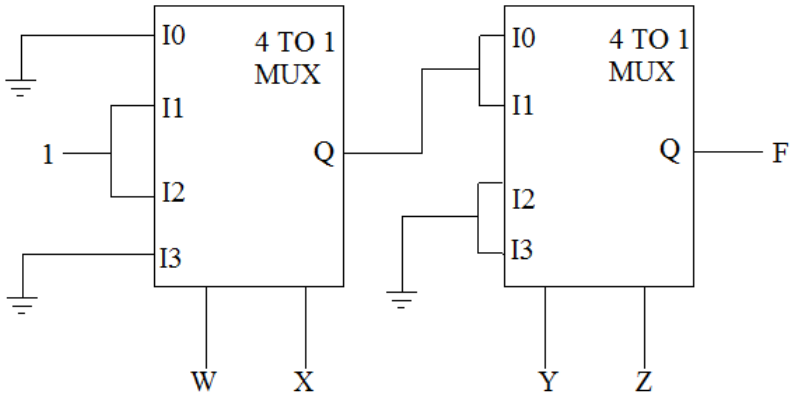
47. In the following circuit X is given by:



(A) $X = A\overline{B}.\overline{C} + \overline{A}B\overline{C} + \overline{A}.\overline{B}C + ABC$
(B) $X = \overline{A}BC + A\overline{B}C + AB\overline{C} + \overline{A}.\overline{B}.\overline{C}$

(C) $X = AB + BC + AC$
(D) $X = \overline{A}.\overline{B} + \overline{B}.\overline{C} + \overline{A}.\overline{C}$

48. In the circuit show below, W and Y are MSBs of the select lines. The output F is given by:

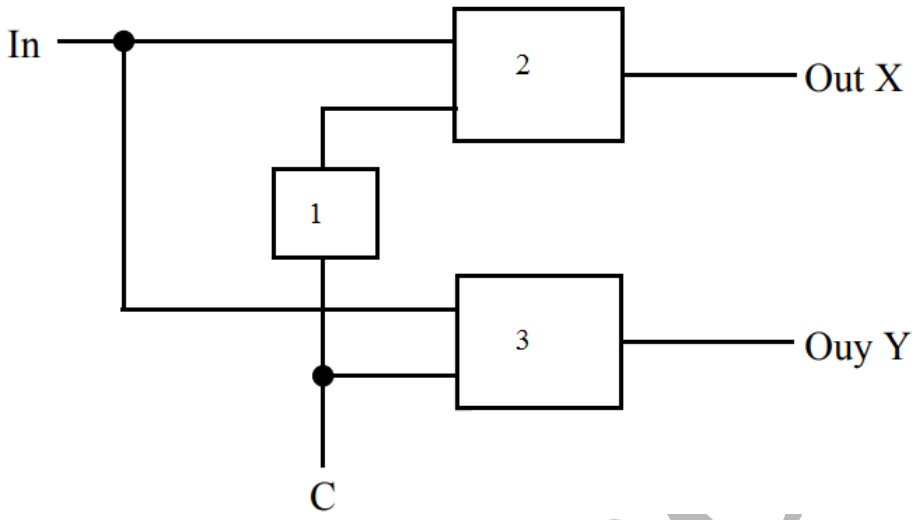


(A) $F = W\overline{X} + \overline{W}X + \overline{Y}.\overline{Z}$
(B) $F = W\overline{X} + \overline{W}X + \overline{Y}Z$
(C) $F = W\overline{X}.\overline{Y} + \overline{W}X\overline{Y}$
(D) $F = (\overline{W} + \overline{X})\overline{Y}.\overline{Z}$

49. Consider the truth table below:

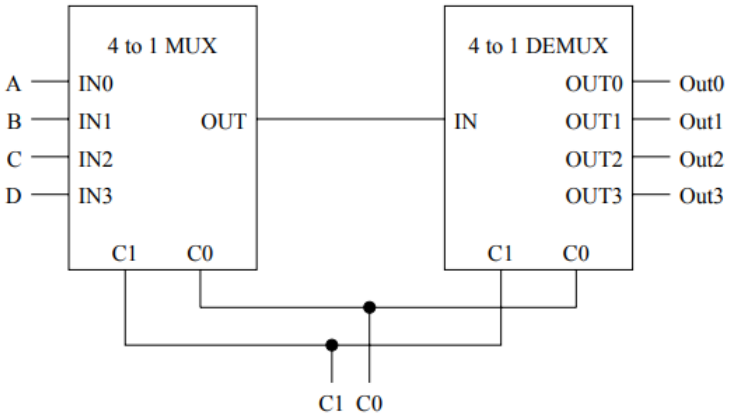
IN	C	Out_A	Out_B
0	0	0	0
1	0	1	0
0	1	0	0
1	1	0	1

The following circuit implements a 1-to-2 demultiplexer as described in the truth table above using basic gates as follows:



Which of the following tuples express the gates used in above circuit as (1,2,3):
(A) (NOT, OR, AND)
(B) (OR, NOT, AND)
(C) (NOT, AND, AND)
(D) (AND, NOT, OR)

50. Consider the circuit shown below and the corresponding truth table.



In_3	In_2	In_1	In_0	C_1	C_0	Out_3	Out_2	Out_1	Out_0
D	C	B	A	0	0				
D	C	B	A	0	1				
D	C	B	A	1	0				
D	C	B	A	1	1				

Which of the following tables represents the output part of the truth table for the circuit shown above. Assume the four inputs to the multiplexer are A, B, C,and D.

(A)

Out_3	Out_2	Out_1	Out_0
0	0	0	A
0	0	B	0
0	C	0	0
D	0	0	0

(B)

Out_3	Out_2	Out_1	Out_0
0	0	0	A
0	0	C	0
0	B	0	0
D	0	0	0

(C)

Out_3	Out_2	Out_1	Out_0
0	0	0	A
0	0	D	0
0	C	0	0
B	0	0	0

(D)

Out_3	Out_2	Out_1	Out_0
0	0	0	C
0	0	D	0
0	A	0	0
B	0	0	0