2 ALU, Datapath and Control Unit

1. Consider an array multiplier for multiplying two n-bit numbers. If each gate in the circuit has a unit delay, the total delay of the multiplier is:
   (A) $O(1)$
   (B) $O(logn)$
   (C) $O(n)$
   (D) $O(n^2)$

2. You are given two implementations of the same Instruction Set Architecture (ISA):
   Machine A, with 2 CPI and 1 ns cycle time.
   Machine B, with 1.2 CPI and 2 ns cycle time.
   Which machine is faster?
   (A) Machine A is 40% faster than machine B.
   (B) Machine B is 30% faster than machine A.
   (C) Machine A is 20% faster than machine B.
   (D) Machine B is 25% faster than machine A.

3. Consider two processors P_1 and P_2 executing the same instruction set. Assume that under identical conditions, for the same input, a program running on P_2 takes 25% more time but incurs 20% less CPI (clock cycles per instruction) as compared to the program running on P_1. If the clock frequency of p1 is 2GHz, then the clock frequency of P_2 (in GHz) is:
   (A) 2.567
   (B) 1.28
   (C) 1.82
   (D) 2.33

4. The size of ROM needed to implement a 8 bit multiplier in a system, which has strict memory alignment implemented, is
   (A) 1 MBytes
   (B) 10 MBytes
   (C) 1 Mbits
   (D) 8 Mbits

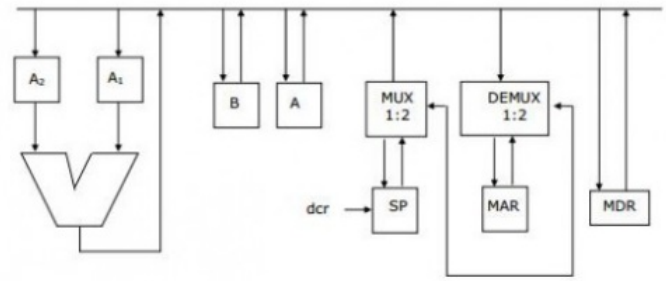
5. The floating point unit of a processor using a design D takes $2t$ cycles compared to t cycles taken by the fixed point unit. There are two more design suggestions D_1 and D_2 . D_1 uses 30% more cycles for fixed point unit but 30% less cycles for floating point unit as compared to design D. D_2 uses 40% less cycles for fixed point unit but 10% more cycles for floating point unit as compared to design D .
   For a given program which has 80% fixed point operations and 20% floating point operations, which of the following ordering reflects the relative

performances of three designs? (where $D_i > D_j$ denotes that D_i is faster than D_j)
(A) $D_1 > D > D_2$
(B) $D_2 > D_1 > D$
(C) $D > D_1 > D_2$
(D) $D_2 > D > D_1$

6. Suppose the functions F and G can be computed in 8 and 3 nanoseconds by functional units U_F and U_G, respectively. Given three instances of U_F and three instances of U_G, it is required to implement the computation $F(G(X_i))$ for $1 \leq i \leq 13$. Ignoring all other delays, the minimum time required to complete this computation is (in nanoseconds):
(A) 29
(B) 39
(C) 34
(D) 40
(E) 43

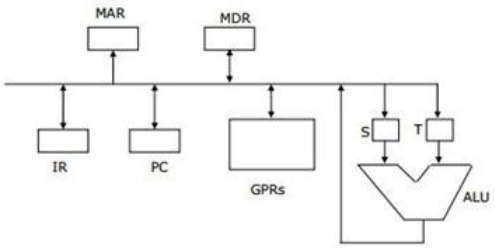
7. Consider the following sequence of micro-operations.
$MBR \leftarrow PC$
$MAR \leftarrow X$
$PC \leftarrow Y$
$Memory \leftarrow MBR$
Which one of the following is a possible operation performed by this sequence?
(A) Instruction fetch
(B) Operand fetch
(C) Conditional branch
(D) Initiation of interrupt service

8. Consider the following data path of a simple non-pipelined CPU. The registers A, B, A_1, A_2, MDR, the bus and the ALU are 8-bit wide. SP and MAR are 16-bit registers. The MUX is of size 8x(2:1) and the DEMUX is of size 8x(1:2). Each memory operation takes 2 CPU clock cycles and uses MAR (Memory Address Register) and MDR (Memory Date Register). SP can be decremented locally.



The CPU instruction "push r" where, (r = A or B) has the hardware level specification as:
$M[SP] \leftarrow r$
$SP \leftarrow SP - 1$
How many CPU clock cycles are required to execute the "push r" instruction?
(A) 2
(B) 3
(C) 4
(D) 5

9. Consider the following data path of a CPU:



The ALU, the bus and all the registers in the data path are of identical size. All operations including incrementation of the PC and the GPRs are to be carried out in the ALU. Two clock cycles are needed for memory read operation: the first one for loading address in the MAR and the next one for loading data from the memory bus into the MDR.
The instruction "$add R_0, R_1$" has the register transfer interpretation $R_0 \Leftarrow R_0 + R_1$. The minimum number of clock cycles needed for execution cycle of this instruction is:
(A) 2
(B) 3
(C) 4
(D) 5

10. Consider following question in context of previous question.

The instruction "call R_n, sub" is a two word instruction. Assuming that PC is incremented during the fetch cycle of the first word of the instruction, its register transfer interpretation is:
$R_n \leftarrow PC + 1$;
$PC \leftarrow M[PC]$;
The minimum number of CPU clock cycles needed during the execution cycle of this instruction is:
(A) 2
(B) 3
(C) 4
(D) 5

11. Microprogrammed control unit:
(A) is faster than a hardwired control unit
(B)facilitates easy implementation of new instructions
(C)is useful when very small programs are to be run
(D)usually refers to control unit of a microprocessor

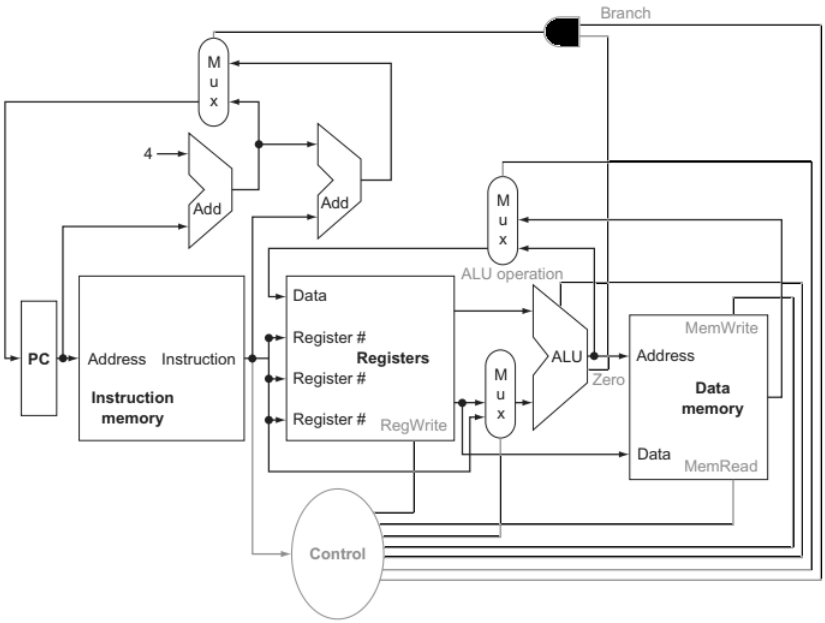
12. Control memory contains all necessary control words required by a processor to execute all of its operations. Which of the following components help in the sequencing of control words in control memory?
(A) Macro-Program counter
(B) Micro-program counter
(C) Control memory address register
(D) Control memory address generator
(E) Control signal handler

13. Match the following:

(X) Micro operation	(1) Sequence of statements stored in control memory.
(Y) Micro instruction	(2) Set of micro-programs.
(Z) Micro program	(3) The way an elementary digital computer does its job.
(W) Micro-code	(4) Statements involving basic computer operation

(A) W-1,X-3,Y-4,Z-1
(B) W-2,X-4,Y-3,Z-4
(C) W-1,X-4,Y-3,Z-2
(D) W-2,X-3,Y-4,Z-4

14. Following three questions are based on the data provided as follows:
Consider the datapath shown below:



In this datapath, Instruction memory, Data Memory, Adder, Multiplexer, ALU, Registers and Control blocks have latencies of 400 ps (pico seconds), 350 ps, 100 ps, 30 ps, 120 ps, 200 ps and 100 ps, respectively.
Consider the addition of a multiplier to the ALU. This addition will add 300 ps to the latency of the ALU. The result will be 5% fewer instructions executed since we no longer need to emulate the MUL instruction.
Note that a cycle time is defined as the time needed to execute an instruction completely. For example, *Load word* loads a word from data memory to one of the data registers in one cycle.
If (p,q) denotes the values of cycle times without and with above mentioned improvement, which of the following represents correct value of (p,q)?
(A) (1130,1630)
(B) (1160,1530)
(C) (1430, 1730)
(D) (1360,1630)

15. Which of the following is true about the speedup achieved in the modified system for 1000 instructions?
(A) A significant speedup of 14% is observed.
(B) A significant drop in speedup of 26% is observed.
(C) A significant speedup of 116% is observed.
(D) A significant drop in speedup of 14% is observed.

16. If the only thing required to be done in the processor (depicted above) is fetching consecutive instructions, what would the cycle time (in ps) be?
(A) 1130
(B) 600
(C) 400
(D) 750

17. Consider an architecture of a processor which is divided in following parts each part performing a spacial job followed by their processing time.
Instruction Fetching component: 250 ps
Instruction Decoding component: 350 ps
Instruction Executing component: 150 ps
Memory Accessing component: 300ps
Register writing component: 200 ps
In this processor following instructions are executed:
lw \$1 100(\$0)
lw \$2 200(\$0)
lw \$3 300(\$0)
There are registers in between any two components to hold the results provided from previous component which has a delay of 10 ps.
If the instructions are executed once in sequence and next time in pipelined manner, what is the difference between the two completion times (in ps)?
(A) 2010
(B) 2019
(C) 1960
(D) 1860
(E) 1740

18. Which of the following is true about fixed-sized opcodes:
(A) The amount of space used is less.
(B) Instruction decode is faster and more efficient.
(C) Control determines the length and position of the opcode in the instruction.
(D) All of the above.

19. A speedup of 50 on half of a program result in an overall speedup of:
(A) at least 2 times
(B) at most 2.5 times
(C) at least 3 times
(D) at most 2 times

20. Consider following statements:
(i) Program execution time increases when the instruction count increases.

(ii) In a load/store architecture, the only instructions that access memory are load and store types.
(iii) More powerful instructions lead to higher performance since the total number of instructions executed is smaller for a given task with more powerful instructions.
(iv) An add operation has 3 operands (2 input and 1 output), therefore add instructions must be 3-address instructions.

Which of the above statement/s is/are not correct?
(A) (i) only
(B) (i) and (ii) only
(C) (i), (ii)and (iii) only
(D) (iii) and (iv) only

21. A compiler designer is trying to decide between two code sequences for a particular machine. The machine supports three classes of instructions: A, B, and C.
Class A takes 3 clock cycle to execute
Class B takes 5 clock cycles to execute
Class C takes 6 clock cycles to execute
We now have two sequences of instructions made up of Class A, B, and C instructions respectively.
Let's assume that:
Sequence 1 contains: 200 A's, 100 B's, and 200 C's.
Sequence 2 contains: 400 A's, 100 B's, and 50 C's
Which sequence is faster by how much and what is the CPI difference?
(A) Sequence 1 is faster by 50%, CPI difference is 1.105
(B) Sequence 2 is faster by 15%, CPI difference is 0.964
(C) Sequence 1 is faster by 25%, CPI difference is 0.867
(D) Sequence 2 is faster by 33.33%, CPI difference is 1.334

22. Two compilers are being tested for a 1 GHz machine with three classes of instructions A, B, and C having 1, 2, and 3 clock cycles respectively.
Compiler 1 is tested for sequence 1 (S_1) with five Millions of type A instructions, one Million of type B instructions and one Million of type C instructions. Compiler 2 is tested for sequence 2 (S_2) ten Millions of type A instructions, one Million of type B instructions and one Million of type C instructions.
Which of the following pairs shows the sequence with higher MIPS rating and the difference in MIPS rating itself, respectively?
(A) $S_1, 100$
(B) $S_2, 100$
(C) $S_2, 200$
(D) $S_1, 200$

23. Consider two different designs of ALU as follows:
(i) A part of a bigger task is improved twenty times than it was before. The other part of the same task constitutes 65% of the overall task time.
(ii) The designer can make changes to improve 72% of the task 80% faster.
Which of the following is true about these two improvements:
(A) (i) is a better modification.
(B) (ii) is a better modification.
(C) (i) is 18% faster than (ii)
(D) (i) is 18% slower than (ii)
(E) None of the above

24. Consider a CPU that executes the following mix of instructions:
43% are ALU operations that take 1 Cycle
21% are Load instructions that take 1 Cycle
12% are Store instructions that take 2 Cycles
24% are Jump instructions that take 2 Cycles
A modification is introduced in order to improve the store instruction to consume only 1 Cycle instead of 2 Cycles but this modification causes the cpu clock to become slower by 15%.
Which of the following correctly shows the effect caused by this modification?
(A) CPU takes 5% less time with changes.
(B) CPU takes 10% less time with changes.
(C) CPU takes 5% more time with changes.
(D) CPU takes 7% more time with changes.

25. Assume that you have the following mix of instructions with average CPIs:
The CPU is operating at a clock of 1 GHz. We want to improve the performance of this machine.

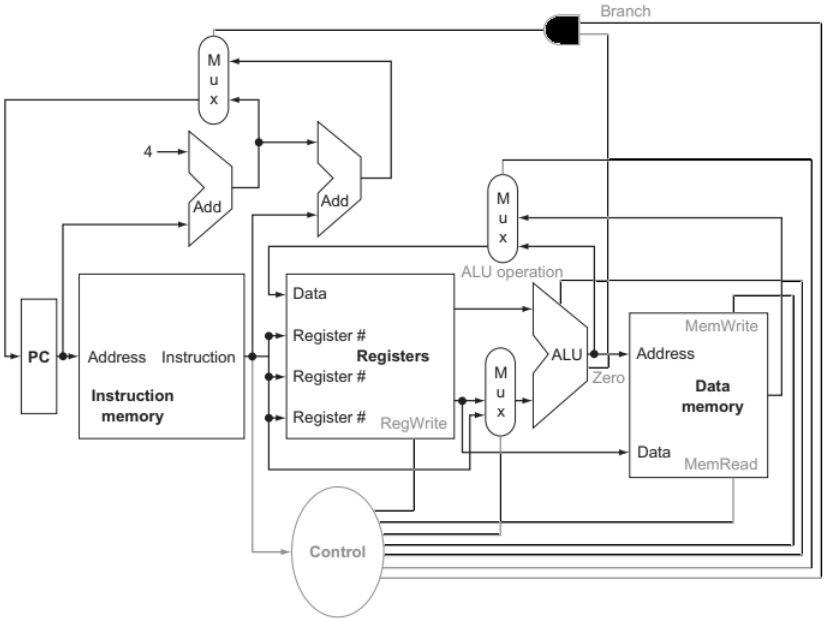
TYPE	**%**	**Average CPI**
ALU	47	6.7
LOAD	19	7.9
BRANCH	20	5
STORE	14	7.1

This machine is to be redesigned. A modified multiplier is incorporated to reduce the average CPI of MUL instructions and the CPI of MUL instructions is dropped by two cycles to six. The percentage of multiplication instructions out of all ALU instructions is 23%.
By how much % will the performance be improved?
(A) 7.25%
(B) 3.37%
(C) 5.67%

(D) 8.03%

26. Consider following three improvements on a processor:
1. 95% of a tasks are improved by 10%
2. 36% of a tasks are improved by 3 times
3. 30% of a tasks are infinitely improved
Let the speedups achieved in case 1, case 2 and case 3 be A, B and C respectively.
Which of the following expressions has the highest decimal value:
(A) $A * |B - C|$
(B) $B * |A - C|$
(C) $C * |A - B|$
(D) $|A - B| * |A - C|$

27. Consider the datapath shown below:



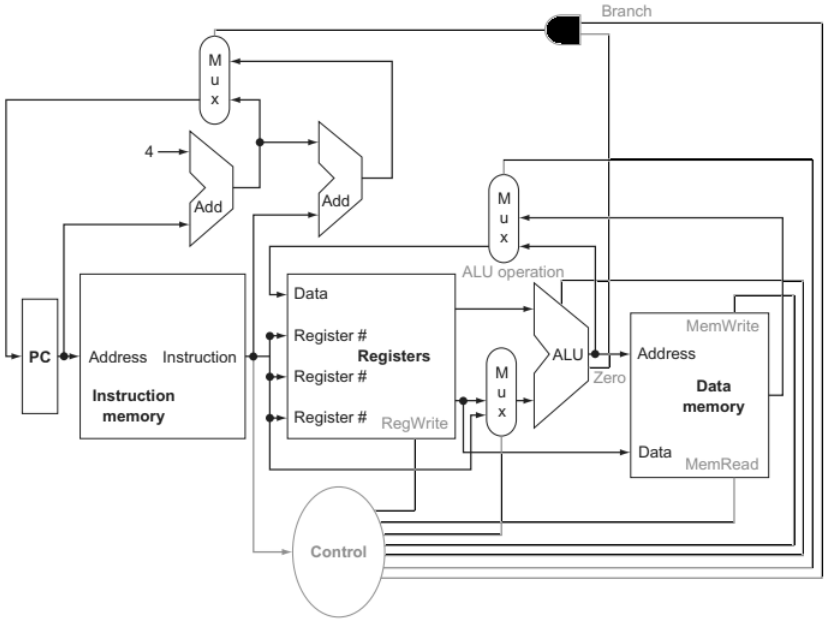
In the above datapath, Instruction memory, Data Memory, Adder, Multiplexer, ALU, Registers and Control blocks have latencies of 400 ps (pico seconds), 350 ps, 100 ps, 30 ps, 120 ps, 200 ps and 100 ps, respectively with a word size of 32 bits.
Note that a cycle time is defined as the time needed to execute an instruction completely.
Consider following instructions (in memory) which are to be executed on this processor:
lw \$*s*0, (3000)

lw \$*s*1, (3008)
sub \$*s*2, \$*s*1, \$*s*0
sw \$*s*2, (4000)

The time needed to execute above instructions (in ns) is:
(A) 40
(B) 4.14
(C) 5.14
(D) 15.54
(E) 16.34

28. Consider the datapath shown in previous question.
If in the sequence of instruction given above the subtraction operation stores the result directly stores the result into data memory in the very next cycle after the computation in ALU (which reduces the instruction count by 1), what is the amount of improvement achieved in time (in ps)?
(A) 4000
(B) 2014
(C) 2019
(D) 1080
(E) 1947

29. Consider the datapath shown below:



In the above datapath, Instruction memory, Data Memory, Adder, Multi-

plexer, ALU, Registers and Control blocks have latencies of 400 ps (pico seconds), 400 ps, 100 ps, 30 ps, 120 ps, 200 ps and 100 ps, respectively with a word size of 32 bits. Note that a cycle time is defined as the time needed to execute an instruction completely.
What is the minimum clock frequency (in MHz) for this processor?
(A) 500
(B) 100
(C) 896.67
(D) 675.7
(E) 1033.33

30. This question is to be seen in the same context as of the previous question.
Consider an improvement is introduced into the ALU by embedding a Floating point unit. Due to this improvement all 35% operations involving float values are evaluated in 40% less time.
What is the speedup achieved with this modification?
(A) 1.01161
(B) 1.05323
(C) 1.16260
(D) 1.67567
(E) 1.03333

31. This question is to be seen in the same context as of the previous question.
The designer of the datapath has to choose only one between the two performance optimizations:
(i) Either a new ALU (with a new latency of 30 ps) or
(ii) A new register file (with a new latency of 160 ps).
Which would be a better choice?
(A) (i) as CPU is more important than registers.
(B) (ii) as registers have greater ratio of optimization which will reduce the cycle time effectively.
(C) (i) as CPU has greater overall impact on cycle time.
(D) (ii) as registers have greater overall impact on cycle time.
(E) None of the optimizations actually introduce any improvement as the overall cycle time is dominated by Memory with a highest delay value.
(F) Both the modifications have same amount of improvement.

32. The content of top of the memory stack (TOS) is 5320. The content of stack pointer SP is 3560. A two-word call sub-routine instruction is located in memory location 1120 followed by the address field 6720 at location 1121.
The content of PC is shown in a tuple format as (a,b,c), where:
(a) Before the call instruction is fetched from memory.

(b) After the call instruction is executed.
(c) After the return from sub-routine.
Which of the following tuples shows the correct values of (a,b,c) for PC ?
(A) (5320,1120,1121)
(B) (1120,6720,1121)
(C) (5320,1120,6720)
(D) (1120,6720,1122)

33. In the context of previous question the values of SP and TOS in (a,b,c) tuple format (as described above), respectively, are:
(A) (3560,3559,3558), (5320,1120,5318)
(B) (5320,5319,5318), (5320,1122,5320)
(C) (5320,5319,5320), (5320,1120,5318)
(D) (3560,3558,3560), (5320,1122,5320)
(E) (3560,3558,3556), (5320,1120,5318)

34. Consider following statements about Horizontal microprogamming:
(i) It does not need signal decoders.
(ii) Word size is smaller when compared to non-horizontal counter-part.
(iii) Number of signals are more when compared to non-horizontal counter-part.
Which of the above statements are correct?
(A) (i) only
(B) (i) and (ii) only
(C) (iii) only
(D) (ii) and (iii) only

35. Consider a CPU where all the instructions require 7 clock cycles to complete execution. There are 140 instructions in the instruction set. It is found that 125 control signals are needed to be generated by the control unit. While designing the horizontal microprogrammed control unit, single address field format is used for branch control logic. What is the minimum size of the control word and control address register?
(A) 125, 7
(B) 125, 10
(C) 135, 9
(D) 135, 10

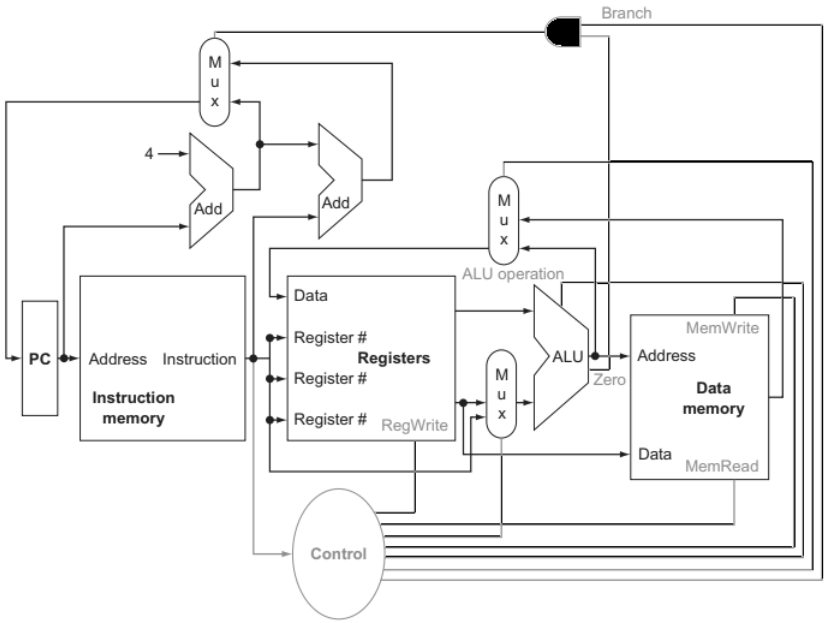
36. A 32 bit system employs a micro program control unit to generate a total of 150 control signals. Assume that during the execution of any of 100 microinstructions, at least 3 control signals and at most 5 control signals are active. The branch address field determines the address as the branch target based on a dozen of different conditions. Minimum number of bits

required in the control word, if 4 miscellaneous bits are there, is:
(A) 40
(B) 44
(C) 51
(D) 55
(E) 63

37. An instruction set of a processor has 266 control signals. These signals operate in 8 mutually exclusive groups as follows:
Group 1 : 38 *signals*,
Group 2 : 75 *signals*,
Group 3 : 46 *signals*,
Group 4 : 10 *signals*,
Group 5 : 30 *signals*,
Group 6 : 18 *signals*,
Group 7 : 25 *signals*,
Group 8 : 24 *signals*,
How many bits of the control words can be saved by using vertical microprogramming over horizontal microprogramming if 14 and 33 additional control bits are employed by horizontal microprogramming and vertical microprogramming respectively ?
(A) 43
(B) 186
(C) 190
(D) 204
(E) 223

Following two questions are based on following data:

38. The latencies of the components of the single-cycle datapath (shown below) are:



Memory Read: 6 ns, Memory Write: 12 ns, Register: 3 ns, ALU: 4 ns, MUX: 1ns (all other components have negligible latency):
If the clock-cycle time is made as small as possible, what is the clock frequency (in MHz)?
(A) 34.44
(B) 38.46
(C) 44.55
(D) 47.47
(E) 55.45

39. We have to choose between two performance optimizations:
(i) A new ALU (latency 3 ns) with new multiplexers (latency 0.5 ns)
(ii) A new register file (latency 1 ns).
Which would be a better choice?
(A) (i) as CPU is more important than registers.
(B) (ii) as registers have greater amount of optimization which will reduce the cycle time effectively.
(C) (i) as CPU has greater overall impact on cycle time.
(D) (ii) as registers have greater overall impact on cycle time.
(E) None of the optimizations actually introduce any improvement as the overall cycle time is dominated by Memory with a highest delay value.
(F) Both the modifications have same amount of improvement.

40. Two teams of Scientists are optimizing an MIPS program for a single-

cycle processor. Team A discovers that by unrolling loops, they increase the static instruction count of the program by 20%, but reduce the dynamic instruction count to 90% of the original value. Team B discovers that a complex data-structure is used by two functions foo() and bar(), which account for 60% and 30% of the running time respectively. By simplifying the data-structure, they are able to make foo() run 1.5 times faster, but bar() now runs 1.2 times slower. Which team has better performance optimization?
(A) Team A
(B) Team B
(C) Both have same amount of improvements
(D) No team has shown any improvement